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ONE APPROACH TO COMPACT TESTING OF DIGITAL CIRCUITS

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A problem of signature analyzer synthesis with required properties is solved for digital schemes compact testing. The main attention is devoted to the issues of eliminating losses of diagnostic information and to simplicity of structural organization. Solutions are based on detecting all error vectors or matrices resulting from failures of diagnostics objects related to the postulated class. Any other error vectors or matrices can be non-detectable and are excluded from consideration. For the compact testing of separate units of complex digital systems, the problem of synthesis of the generator structure that reproduces an assigned sequence of binary sets is being solved. Increased attention is given to issues of the non-excessive reproduction of sets sequence and structural organization simplicity. The solution is based on the application of a mathematical tool for linear sequence machines. A software implementation of the mathematical model is proposed. Error vectors or matrix detection process visualization aids are given. Additionally, means of the binary sets generation process visualization are presented.

Key words: Vector, Tests, Synthesis, Sequencing, Matrices, Digitization, Compactness, Approach

INTRODUCTION

Self-testing of diagnostics objects (DO) is a maximally self-contained method of embedded diagnostics testing, because the generation of test inputs and analysis of the results of test information are not supported by the system facilities [1]. Actually, any self-testing method is based on test impacts generation and compact representation of test impact passage results. Therefore, the problem of sound selection of embedded equipment parameters is essential for any DO manufacturing process [2-3].

Currently the need for cost-effective testing systems is increasing due to the enhanced level of integration of computing equipment component base. Therefore, the trend toward decreasing the complexity of diagnostic facilities hardware exists. Built-in test aids are of great importance, for example, in large and extra-large integrated circuits development [3-4].

The methodology of digital systems diagnosis based on transformation of binary sequences coming to the DO into compact specifications -- signatures, comparison of obtained signatures with reference signatures, and corresponding processing of comparison results -- are the essence of signature analysis [5-7]. As a rule, mathematical tools from antinoise coding theory are used as a theoretical apparatus for signature analyzer development. However, theoretical substantiation of the development of hardware signature analyzers (SA) with required properties is most advantageous when based on the mathematical tools of linear sequential machines (LSM) [8-9].

A classical signature analyzer is in principle unable to detect all possible combinations of errors. Some part of them will never appear at the DO output, and therefore there is no need to detect them. The following task is posed in this paper: to build a simple signature analyzer that would detect all DO errors caused by the faults from the postulated class.

A control test, especially when dealing with limited time dedicated to the control, is a "mixture" of pseudo-random and deterministic sets of test impacts. Hardware for the generation of pseudo-random sets is well known, and there are no serious problems in their implementation [10-11]. However, the storage of the deterministic part of a check test in read-only memory, as a rule, is not always acceptable, because it is related to significant hardware requirements. In conjunction with this, the task of creating simple hardware that reproduces assigned binary sets sequence that compose the deterministic part of the check test arises.

A LINEAR SEQUENTIAL MACHINE AS A SIGNATURE ANALYZER

Processes in LSM with *l* -inputs, *m* -outputs, and n -memory elements (Figure 1) are described by linear system of state equations and linear system of output equations, which appear as follows in matrix form:

$$S^{t+1} = AS^t + BU^t$$

$$Y^t = CS^t + DU^t$$

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where

$$A=\left\|a_{ij}\right\|_{n\times n}, B=\left\|b_j\right\|_{n\times l}, C=\left\|c_j\right\|_{m\times n}, D=\left\|d_j\right\|_{m\times l}$$

the characteristic matrices, in which elements in behavior equations are presented in a Galois field GF(2).

Input U^t, output, Y^t and S^t LSM state at a time moment t are specified in the form of corresponding column vectors

$$U^t=\left\|u_i^t\right\|_l, Y^t=\left\|y_i^t\right\|_m, S^t=\left\|s_i^t\right\|_n$$

The structure of LSM is described by the matrix of the connection A of memory elements, in which every element a_{ij} is defined as follows:

$a_{ij} = 1$, if the output of the j-th memory element is connected to the input of the i-th memory element;
$a_{ij} = 0$, otherwise.

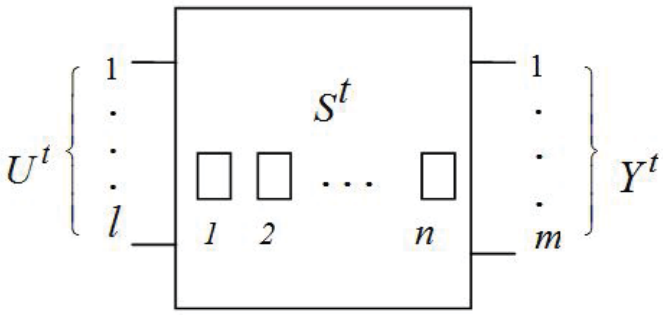

Figure 1: The structure of a linear sequential machine

Other matrices can be interpreted similarly, matrices which set links between inputs and memory elements (B), between memory elements and outputs (C), and between inputs and outputs (D).

It is expedient to implement the analysis of DO responses l with the outputs for test input under conditions of limited resources for additionally introducing hardware, by connecting LSM l with inputs (Figure 2), and this will serve as the signature analyzer.

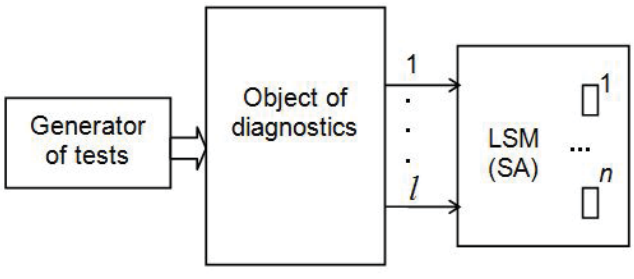

Figure 2: Diagnostics object with signature analyzer

When DO testing is complete, SA memory element states will be equal to modulo two sum of the reference signature R_{st} and R_{er} error signature $R_{st} + R_{er}$. At that, a failure will be revealed if $R_{er} \neq 0$.

A method of deriving signatures and proof of the effectiveness of their use are essential here, i.e. the possibility of detecting errors with an acceptable probability after compression of binary sequences. It is known that the probability of not detecting an error P_{ud} in a sequence of interchangeable logical states at DO output ($l = 1$) is equal to [09]:

$$P_{ud}=\frac{2^{N-n}-1}{2^N-1}$$

where N - is the length of the sequence, n - is the number of SA digits ($N >> n$). In other words, compressing a long sequence into a short signature is associated with diagnostics information loss.

It is proposed to exclude recognition ambiguity inherent to compact testing, as follows. It is necessary to build LSM that detects the entire set of error vectors ($l = 1$) or matrices ($l \geq 2$) of DO response to the control test which are caused by the specification of failures from the postulated class. Of course, there is no need to reveal vectors or matrices of errors which cannot appear at DO outputs in principle.

A SIGNATURE ANALYZER WITH REQUIRED PROPERTIES

Let there be an l-output digital network, and a sequence of tests consisting of N binary sets comprising a full test for it, i.e., ensuring the appearance of any fault from the postulated class at the network outputs

$$S=\{s_\nu\},\ \nu=\overline{1,M}.$$

Let us name the matrix of the v-th error caused by a fault $s_v \in S$ as

$$E^\nu=\left[e_j^\nu\right]\ \ i=\overline{1,l};\ \ j=\overline{0,N-1}$$

in which each element e_{ij}^ν is defined as follows:

$e_{ij}^\nu = 0$, if at the j-th set of input sequence the object response that is in the v-th technical state, coincides with a reference response at the i-th output;

$e_{ij}^\nu = 1$, otherwise.

An error vector is a special case of an error matrix when *l = 1*. Let's represent error matrix also in the following form:

$$E^{\nu} = \left| E^{\nu}_{N-1} E^{\nu}_{N-2} ... E^{\nu}_{j} ... E^{\nu}_{0} \right| ,$$

where

$$E^{\nu}_{j} = \left| e^{\nu}_{1j} \quad ... \quad e^{\nu}_{j} \quad ... \quad e^{\nu}_{j} \right|^{T}, \; j = \overline{0, N-1} .$$

A task solving algorithm includes steps which description is essentially a proof of the justifiability of ideas laid out as the basis of the suggested approach:

1. We shall present $E^{\nu}, \nu = \overline{1, M}$ matrices in a vector form using conjugation ε^{ν} by columns operation, in such a manner that E^{ν}_{j} transforms into $E^{\nu^T}_{j}$ for all $j = \overline{0, N-1}$ (the process is shown at Figure 3)

$$\varepsilon^{\nu} = \left| E^{\nu^T}_{N-1} E^{\nu^T}_{N-2} ... E^{\nu^T}_{j} ... E^{\nu^T}_{0} \right|, \; \nu = \overline{1, M}.$$

As a result, the vectors ε^{ν} take the form

$$\varepsilon^{\nu} = \left| e^{\nu}_{l(N-1)} \; e^{\nu}_{(l-1)(N-1)} \; ... \; e^{\nu}_{1} \; e^{\nu}_{0} \right|, \; \nu = \overline{1, M} .$$

2. We shall search for a polynomial
$\xi_0(x) = x^n + C_1 x^{n-1} + ... + C_n$
of degree *n* that is not a divider of polynomials

$$e^{\nu}_{l(N-1)} + e^{\nu}_{(l-1)(N-1)} \cdot x + ...$$
$$... + e^{\nu}_{1} \cdot x^{(N-2)} + e^{\nu}_{0} \cdot x^{(N-1)}, \; \nu = \overline{1, M}$$

of vectors ε^{ν}.

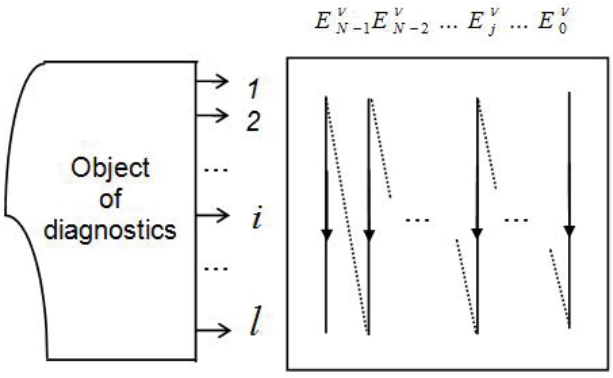

Figure 3. Principle of vector formation ε^{ν}

The polynomial $\xi_0(x)$ is searched for by simple enumeration, starting from the simplest polynomial *x+1* of degree *n = 1* until the required nondivisibility condition is met.

3. We construct for the polynomial $\xi_0(x)$ an accompanying matrix

$$A_{\xi_0(x)} = \begin{vmatrix} C_1 & C_2 & ... & C_{n-1} & C_n \\ 1 & 0 & ... & 0 & 0 \\ 0 & 1 & ... & 0 & 0 \\ 0 & 0 & ... & 1 & 0 \end{vmatrix}$$

and a column vector $B = \left| 1 \quad 0 \quad ... \quad 0 \right|^{T}$ which fully characterizes a single channel LSM. It is evident that the accompanying matrix $A_{\xi_0(x)}$, which sets links between memory elements, describes an LSM, to which a feedback shift register corresponds.

At that, it should be remembered that $\xi_0(x)$ is a characteristic polynomial of $A_{\xi_0(x)}$ matrix, i.e.

$$\xi_0(x) = \det \left| A_{\xi_0(x)} + x \cdot \mathrm{I} \right|$$

A single channel LSM feedback polynomial
$g(x) = 1 + C_1 + ... + C_n x^n$ is related to $\xi_0(x)$ as follows $g(x) = \xi_0\left(\frac{1}{x}\right) x^n$.

4. We compute the characteristic matrices of the *l*-th channel analog of a single-channel LSM (for *l = 1* the equalities $\overline{A} = A$ and $\overline{B} = B$ are true), which possesses completely the same properties as the single-channel LSM:

$$\overline{A} = A^{l}_{\xi_0(x)} ,$$
$$\overline{B} = \left| A^{l-1}_{\xi_0(x)} \cdot B \quad ... \quad A_{\xi_0(x)} \cdot B \quad B \right| .$$

The detailed argumentation of these relations is given in [08].

Matrices *C* and *D* are of no principal significance for signature analysis and are not considered here.

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5. We shall synthesize an *l*-channel LSM which is described by the characteristic matrices $\overline{A} = \left\| \overline{a}_{ij} \right\|_{n \times n}$ and $\overline{B} = \left\| \overline{b}_{ij} \right\|_{n \times l}$, that will be an SA with the required properties.

Example: The complete verification test for double digital selector-multiplexor *SN74153N* includes the following sets:

$$H_8 = \begin{array}{c|cccccccc|c} & Y(0) & Y(1) & Y(2) & Y(3) & Y(4) & Y(5) & Y(6) & Y(7) & \\ a & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 1 & \rho_1 \\ b & 1 & 0 & 1 & 1 & 0 & 1 & 0 & 0 & \rho_2 \\ c & 0 & 1 & 1 & 0 & 1 & 1 & 0 & 0 & \rho_3 \\ d & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & \rho_4 \\ e & 1 & 1 & 0 & 1 & 0 & 0 & 0 & 1 & \rho_5 \\ f & 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 & \rho_6 \end{array}.$$

Let's build a signature analyzer for *SN74153N* that detects 18 error vectors conditioned by 22 single constant faults:

1. 10000000
2. 01000000
3. 00100000
4. 00010000
5. 00001000
6. 00000100
7. 00000010
8. 00000001
9. 11110000
10. 00110011
11. 11001100
12. 00000110
13. 00001111
14. 01100000
15. 00010010
16. 01001000
17. 10010110
18. 01101001.

The complete DO test is built using the Rot *d*-algorithm, and these error vectors are obtained using digital simulation with introduction of possible faults [14].

So, we find a characteristic polynomial

$\xi_0(x) = x^4 + x + 1$, to which a feedback polynomial $g(x) = 1 + x^3 + x^4$ corresponds, and build a matrix

$$A_{\xi_0(x)} = \begin{vmatrix} 0 & 0 & 1 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \end{vmatrix}.$$

Using matrices $\overline{A} = A_{\xi_0(x)}$ and $\overline{B} = \left| 1 \quad 0 \quad \ldots \quad 0 \right|^T$, we build a single-channel SA (Figure 4) that detects all error vectors caused by the faults from the postulated class without exceptions.

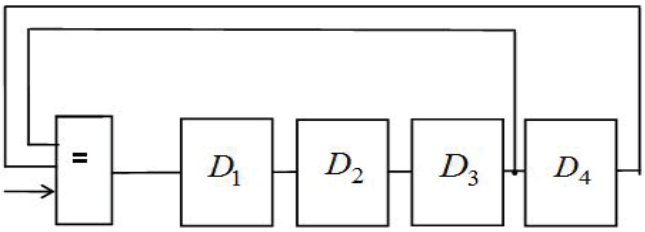

Figure 4: Signature analyzer for SN74153N

AN AUTONOMOUS LINEAR SEQUENCE MACHINE AS A BINARY SETS SEQUENCE GENERATOR

In [12], it was proposed to use LSM which under the impact of a special control sequence generates an assigned binary sets sequence. In this process, excessive intermediate sets appear at the output of LSM that have to be masked. In [13] a register of shift with non-linear feedback function is composed. However, even in this case it is not possible to get rid of excessive intermediate sets.

An autonomous linear sequence machine (ALSM), whose state does not depend on input impacts, is traditionally used for the creation of pseudo-random binary sets sequence. In this work, the following task is set up: to use ALSM as a simple generator that will be able to reproduce an absolutely precisely assigned binary sets sequence forming check test.

Processes in ALSM with *m*-outputs and *n*-memory elements (Figure 5) are described by the linear system of state equations and a linear system of equations of outputs that in matrix form look as follows:

$S^{t+1} = AS^t$
$Y^t = CS^t$

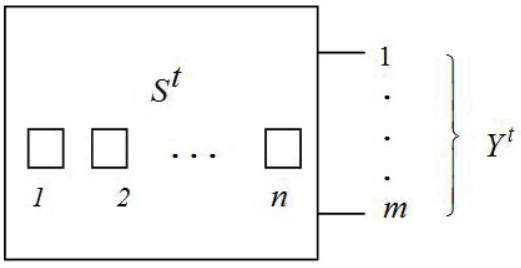

Figure 5: The structure of an autonomous linear sequence machine (ALSM)

THE SYNTHESIS OF A BINARY SETS SEQUENCE GENERATOR

The considered method of the synthesis of a binary sets assigned sequence generator

$$H_n = |Y(0) \quad Y(1) \quad ... \quad Y(n-1)|$$

consists of the following. It is necessary to find such a polynomial

$$\xi(x) = x^r + g_{r-1}x^{r-1} + ... + g_0$$

of a minimal degree $r \le n$, that columns H_n, starting with Y_r, could be presented by the same linear combination of previous r columns. Analytically, it could be presented in the following way:

$$Y(j) = g_{r-1}Y(j-1) + g_{r-2}Y(j-2) + ...$$
$$... + g_0 Y(j-r),\ j = \overline{r,n}.$$

The characteristic matrices of the sequence generator H_n that shift register with feedback $g_{r-1}, g_{r-2}, ..., g_0$ and original state $S^0 = |1 \quad 0 \quad ... \quad 0|^T$, will look like:

$$A = \begin{vmatrix} g_{r-1} & g_{r-2} & \cdots & g_0 \\ 1 & 0 & ... & 0 \\ 0 & 1 & ... & 0 \\ ... & ... & ... & ... \\ 0 & 0 & ... & 10 \end{vmatrix},$$

$$C = H_r F_r^{-1} = H_r \begin{vmatrix} a_1^0 & a_1^1 & ..... & a_1^{r-1} \\ 0 & a_1^0 & ... & a_1^{r-2} \\ 0 & 0 & ... & a_1^{r-3} \\ ... & ... & ... & ... \\ 0 & 0 & ... & a_1^0 \end{vmatrix}^{-1}$$

where $a_1^i = \sum_{j=1}^{i} a_1^{i-j} g_{r-j},\ a_1^0 = 1,\ g_{r-j} = 0$ at $r - j < 0$.

The consequence is that determined in the following way:

$$H_r = |Y(0) \quad Y(1) \quad ... \quad Y(r-1)| =$$
$$= C \cdot |A^0 \cdot S^0 \quad A^1 \cdot S^0 \quad ... \quad A^{r-1} \cdot S^0| = C \cdot F_r.$$

In a number of cases the inverse matrix F_r^{-1} could be calculated in a more simple way:

$$F_r^{-1} = \begin{vmatrix} d_1^0 & d_1^1 & ..... & d_1^{r-1} \\ 0 & d_1^0 & ... & d_1^{r-2} \\ 0 & 0 & ... & d_1^{r-3} \\ ... & ... & ... & ... \\ 0 & 0 & ... & d_1^0 \end{vmatrix}$$

where $d_1^i = \sum_{k=0}^{i-1} d_1^k a_1^{i-k},\quad d_1^0 = 1, i = \overline{1, r-1}.$

In a worst case scenario, when it is not possible to find the linear combination mentioned above, a polynomial $\xi(x)$ will look like $\xi(x) = x^n$, and the generator of an assigned sequence will be n-bit shift register without feedback connections.

Example (continued): It is needed to make ALSM that reproduces assigned binary sets sequence.

Let us transform the matrix H_8 by lines to canonical form H_{can}[15]:

$$H_{can} = \begin{array}{c} \begin{matrix} 0 & 1 & 2 & 3 & 4 & 5 & 6 & 7 \end{matrix} \\ \left|\begin{matrix} 1 & 0 & 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 1 & 0 & 1 & 1 & 1 \\ 0 & 0 & 0 & 0 & 1 & 0 & 0 & 1 \end{matrix}\right| \end{array} \begin{matrix} \rho_1 + \rho_3 + \rho_4 \\ \rho_3 + \rho_6 \\ \rho_2 + \rho_3 + \rho_4 + \rho_6 \\ \rho_1 + \rho_6 \\ \rho_2 + \rho_3 + \rho_4 \end{matrix}$$

H_{can} must meet the requirements:

- not to contain zero lines (linear dependant lines are transformed in zero ones);
- the first one in each line must be located on the right from the first one of the previous line;
- in each column containing such a unit, the remaining elements are equal to zero, if they are located below this one.

In this case, H_{can} has the appearance typical for this particular case, because the first five columns of the matrix H_{can} are linear independent.

In matrix H_{can} in the lower line the first one is in column number four. Consequently, the lower limit of the digit capacity of ALSM in search is equal to five.

The column number five is presented in the form of a linear combination of the five previous ones

Y(5) = Y(3) + Y(2) + Y(0).

However *Y(6) ≠ Y(4) + Y(3) + Y(1)*.

Consequently, we construct the linear combination dependence of the column number six from the six previous ones *Y(6) = Y(3) + Y(2) + Y(1)*, because the fifth column is no longer expressed through the previous columns. This relation stays in power also for column number seven *Y(7) = Y(4) + Y(3) + Y(2)*.

That's why the polynomial in a search takes the form

$$\xi(x) = x^6 + x^3 + x^2 + x^1.$$

Feedback coefficients of the shift register in accordance with $\xi(x)$ is set as follows:

$$g_5 = 0, g_4 = 0, g_3 = 1, g_2 = 1, g_1 = 1, g_0 = 0.$$

And finally, we calculate the matrix of relations of the ALSM outputs with delay elements

$$C = H_6 F_6^{-1} = \begin{vmatrix} 0 & 0 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 & 0 & 1 \\ 0 & 1 & 1 & 0 & 1 & 1 \\ 1 & 1 & 0 & 1 & 0 & 0 \\ 1 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 \end{vmatrix} \times \begin{vmatrix} 1 & 0 & 0 & 1 & 1 & 1 \\ 0 & 1 & 0 & 0 & 1 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{vmatrix} = \begin{vmatrix} 0 & 0 & 1 & 1 & 1 & 1 \\ 1 & 0 & 1 & 0 & 1 & 1 \\ 0 & 1 & 1 & 0 & 0 & 1 \\ 1 & 1 & 0 & 0 & 0 & 0 \\ 1 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 1 & 0 \end{vmatrix}.$$

Synthesized an autonomous linear sequence machine is presented in Figure 6.

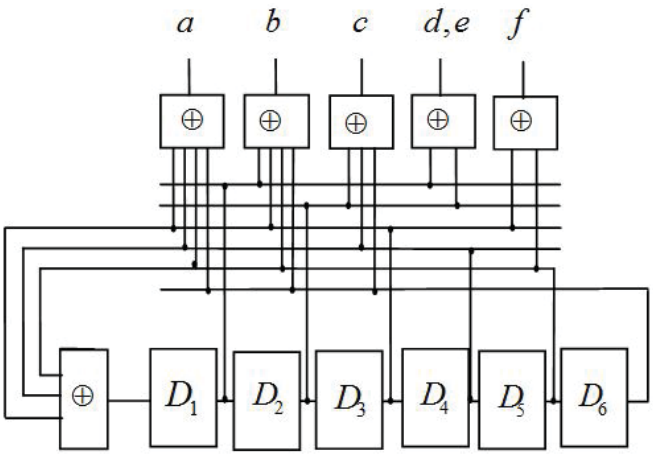

Figure 6. Tests generator for IC TI SN74153N

VISUALIZATION OF THE SIGNATURE ANALYZER AND GENERATOR OPERATING PROCESS

The software implementation of mathematical models of DO with arbitrary configuration and structure (Figures 7 and 8), which was developed by the author in the DELPHI 7.0 programming environment using the hypertext help systems on-line documentation HTML Help Workshop, confirms the validity of the functioning of the developed algorithms.

Screen forms of SA synthesis and generator for final results for digital networks derived using the software model are shown at Figures 9 and 10 for illustration purposes.

Step-by-step observation of error vectors or error matrix detection process in the software model allows assuring visually that the terminal state of SA memory elements differs from the null state, i.e. $R_{er} \neq 0$.

A step-by-step observation of binary sets generation in the program model allows a visual confirmation of this process.

CONCLUSIONS

Thus, the algorithm developed for building a signature analyzer that detects all faults from the postulated class permits synthesis of single-channel and multi-channel LSM structures that are simple in implementation, and free from ambiguity in identification of the technical state of diagnostics objects.

Consequently, the developed algorithm of constructing ALSM reproducing assigned test sets sequence does not require the construction of a special controlling sequence and does not generate the need for excessive sets.

Together, these two approaches make it possible to implement one of the most efficient methods of built-in compact testing of separate components of complicated digital systems.

Furthermore, technical implementation of a diagnostics process using signature analysis with required properties of complex digital systems becomes fairly simple. This fact allows to decrease substantially the requirements for testing staff proficiencies, and to reduce significantly the total tests cost.

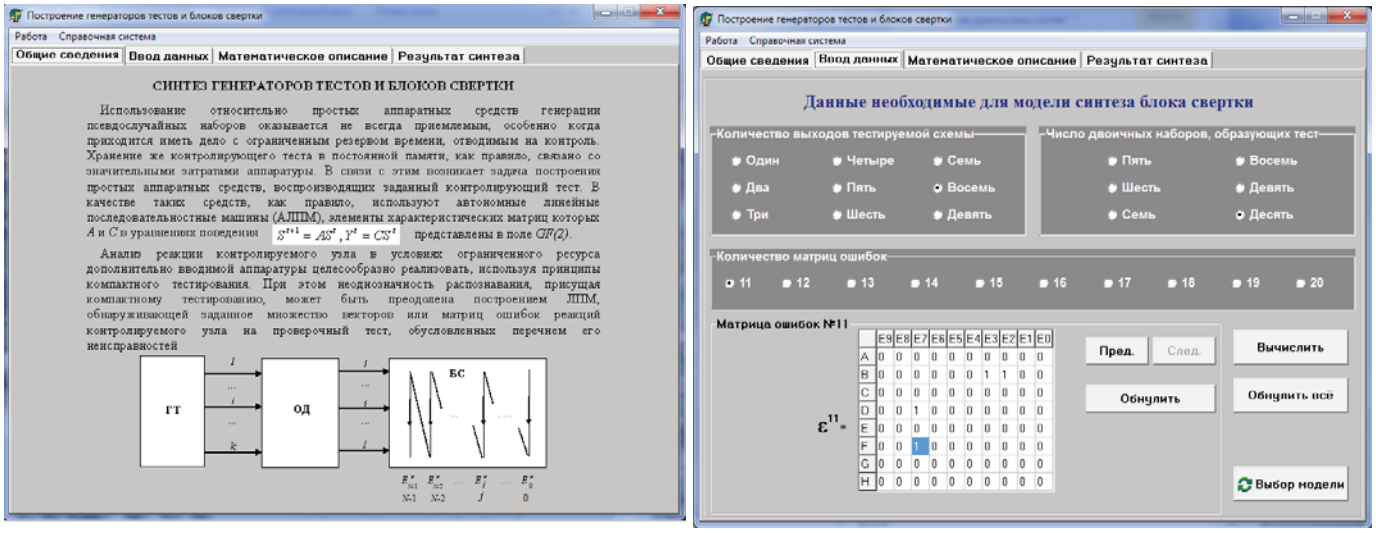

Figure 7: Screen forms of a signature analyzer software model

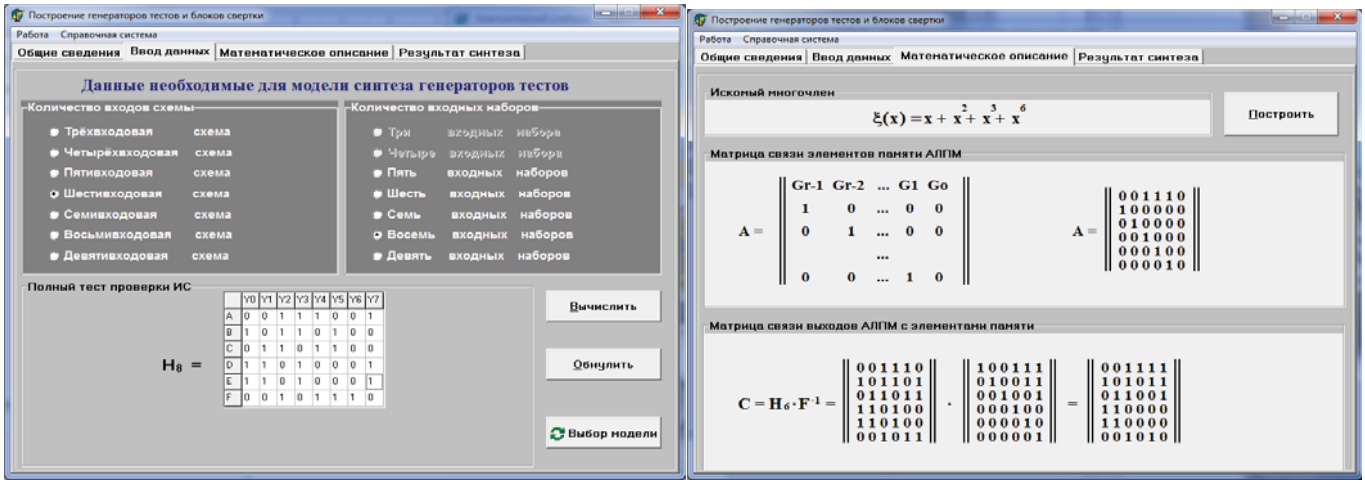

Figure 8: Screen forms of a signature analyzer software model

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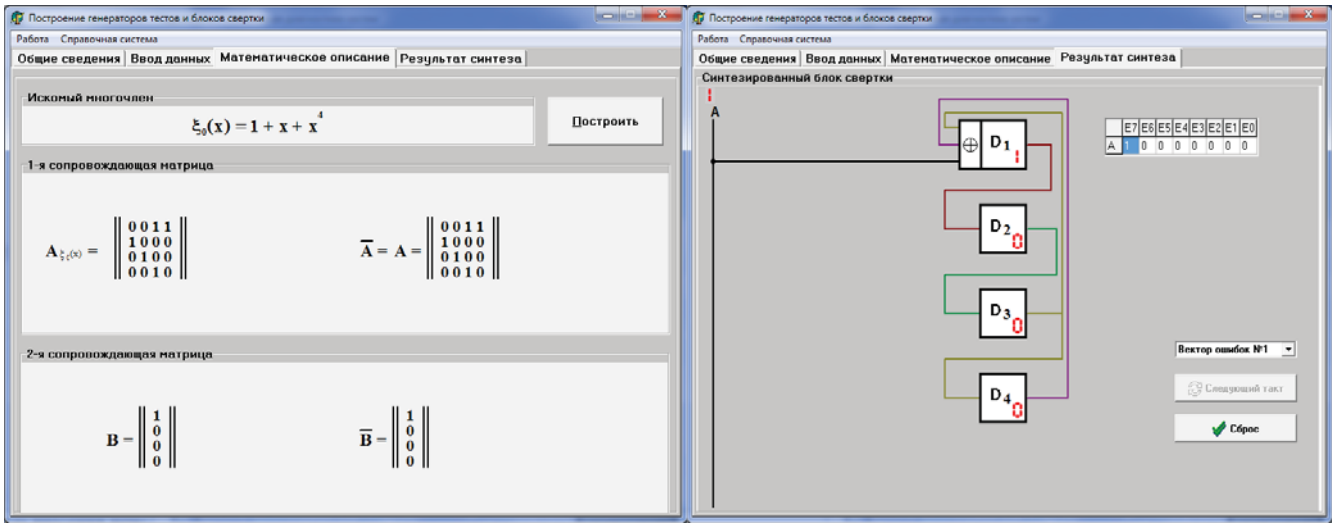
a)



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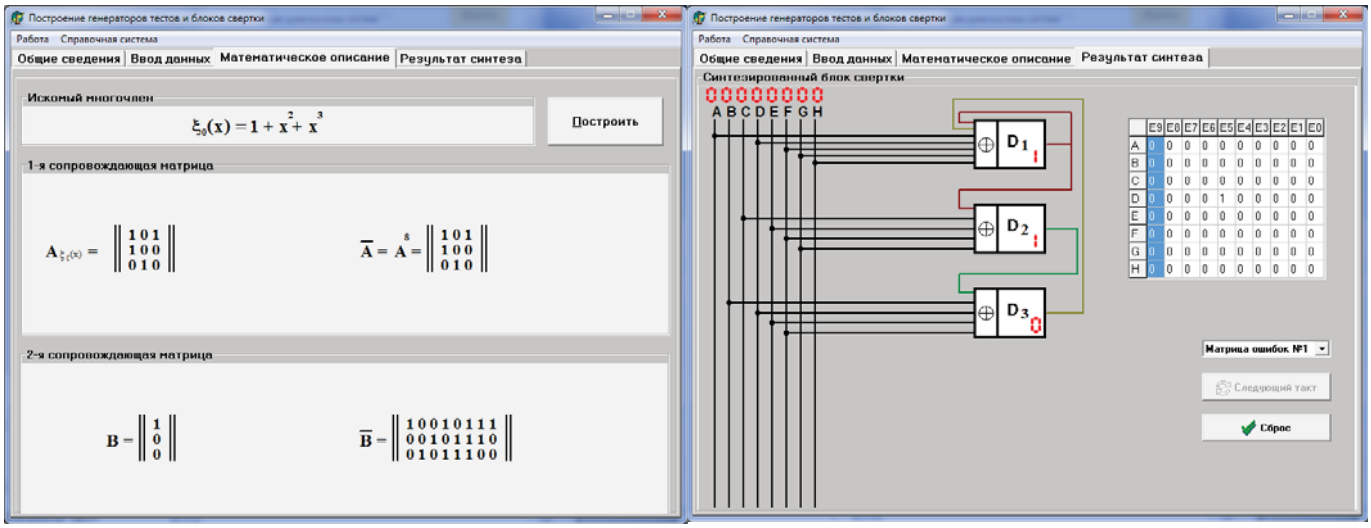

Figure 9: Results of the synthesis of a signature analyzer structure: a - single-channel SA; b - multi-channel SA

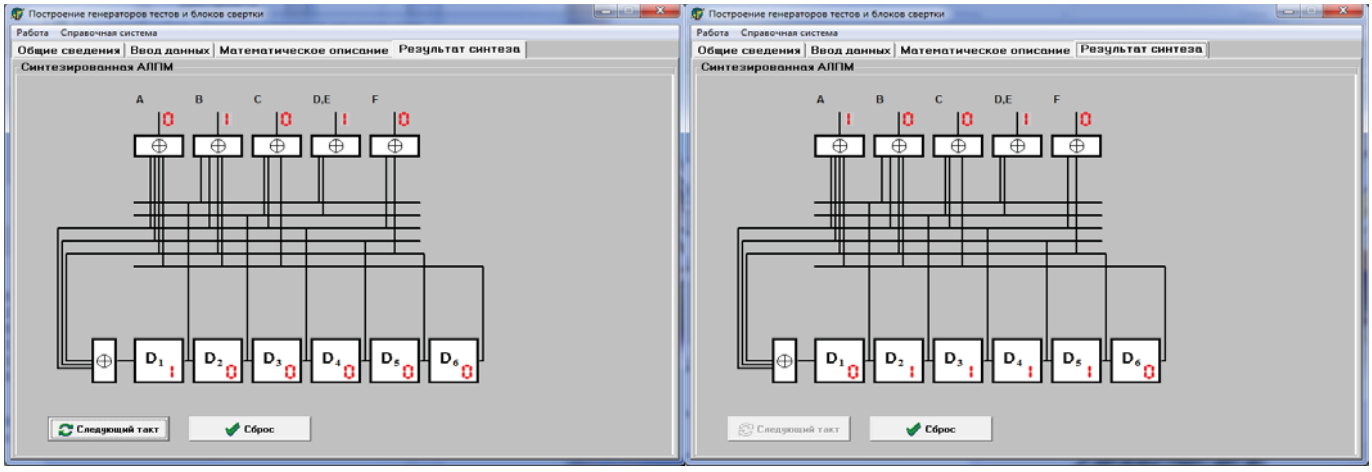

Figure 10: Results of the synthesis of a generator structure

REFERENCES

1. Goryashko A.P. Sintez diagnostiruemyh skhem vychislitel'nyh ustrojstv [Synthesis diagnosed circuits computing devices] / A.P. Goryashko. – M.: Nauka [The science], 1987, p. 288.
2. Brglez F., "On Testability Analysis of Combinational Networks," in Proc. of the International Symp. on Circuits and Systems, May 1984, pp. 220 -225.
3. Khade R., Gourkar S. "Fault Testing of CMOS Integrated Circuits Using Signature Analysis Method," International Journal of Application or Innovation in Engineering & Management (IJAIEM), Vol. 2, Issue 5, May 2013, pp. 73-82.
4. Litikov I.P. Kol'cevoe testirovanie cifrovyh ustrojstv [Circuit testing of digital devices]/ I.P. Litikov.– M.: Energoatomisdat, 1990. p.157.
5. Goessel M., Chakrabarty K., Ocheretnij V. "A Signature Analysis Technique for the Identification of Failing Vectors with Application to Scan-BIST," Journal of Electronic Testing: Theory and Applications, vol. 20, 2004, pp. 611–622.
6. David R., "Signature Analysis of Multi-Output Circuits," in Proc. of the International Fault-Tolerant Computing Symp., June 1984, pp. 366-371.
7. Kinoshita K. and Saluja K.K., "Built-In Testing of Memory Using an On-Chip Compact Testing Scheme, " IEEE Trans. on Computers, vol. C-35, no. 10, Oct. 1986, pp. 862-870.
8. Gill A. Linejnye posledovatel'nostnye mashiny. Analiz, sintez i primenenie [Linear Sequential Circuits. Analysis, Synthesis and Applications]: Per. s angl. / Pod red. [Trans.with Eng./Ed.] Y. Z. Cypkina. – M.: Nauka, 1974, p. 288.
9. Berezkin E.F., "Design of signature analyzer structures with required properties," ARPN Journal of Engineering and Applied Sciences. Volume 13, Number 8, 2018, p. 2850-2854.
10. Hassen S.Z. and McCluskey E.J., "Increased Fault Coverage Through Multiple Signatures," in Proc. of the International Fault-Tolerant Computing Symp., June 1984, pp. 354 -359.
11. Ahmad A, Al-Abri D. Adding pseudo-ran¬dom test sequence generator in the test simulator for DFT approach, Journal of Computer Technology and Applications (JCTA), vol 3(7), 2012, pp. 463–470.
12. Baida I.P., Semerenko V.P., Sintez linejnoj posledovatel'nostnoj mashiny, vosproizvodjashhej zadannuju posledovatel'nost' dvoichnyh naborov [Synthesis of a linear sequential machine that reproduces a given sequence of binary sets]. – Jelektronnoe modelirovanie [Electronic modeling]. 1981, No. 5, pp, 65-70.
13. Daehn W.,Mucha J. Hardware test pattern generation for built-in testing. Intern Test Conf. Philadelphia, 1981, oct., pp.110-113.
14. Berezkin E.F. Nadezhnost' i tekhnicheskaya diagnostika sistem: Uchebnoe posobie [Reliability and technical diagnostics systems: The manual]/ E.F. Berezkin. – M.: NRNU MEPhI, 2012. Ser. Biblioteka jadernogo universiteta [The library of nuclear university], p.244.
15. Lancaster P. and Tismenetsky M., The theory of matrices. New York: Academic Press, 1985, p. 570.

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